

IBM Researchers Advance the Understanding of Chip Reliability at IEEE International Reliability Physics Symposium

ALBANY, N.Y., April 3, 2017 [PRNewswire/](#) -- IBM (NYSE:[IBM](#)) semiconductor and technology researchers will present five papers on the technical and material advancement of its next-generation chip development, including the 7 nanometer node, at the [IEEE International Reliability Physics Symposium](#) (IRPS), April 4-6, 2017.

In pursuit of a mass-manufacturable 7nm chip, and beyond, the IBM team will present papers illustrating progress across:

- insulator material to improve chip operation voltage;
- techniques to model Line Edge Roughness (LER) variation in the spacing between wires on a chip, which impacts voltage;
- techniques for optimal pre-screening of chip tests to better measure failure rates;
- and compare frequency, voltage, time, and temperature dependence of transistor voltage instability in traditional silicon-channel Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) and new Silicon Germanium (SiGe)-channel devices.

The paper, *Time Dependent Dielectric Breakdown of SiN, SiBCN and SiOCN spacer dielectric* presents a comprehensive comparison of several materials that are used for the insulator in the space between the electrical contacts at the transistor level. These spacer dielectrics are some of the thinnest insulators in the chips – tested at 10nm for a 22nm chip, and at about 6nm in a 7nm chip. Understanding how the lifetime of these materials depend on the chip operation voltage is crucial.

"At the 7nm node, parasitic capacitance is projected to increase to 85 percent of device capacitance for the traditional Silicon Nitride (SiN) spacer. We need to find a material that has lower dielectric constant than SiN and is compatible with CMOS integration. [Our paper demonstrates that] Silicon-Boron-Carbon-Nitride (SiBCN) and Silicon-Oxygen-Carbon-Nitride (SiOCN) meet these requirements," said James Stathis, Manager, Electrical Characterization and Reliability, IBM Research.

IBM has implemented SiBCN in 14nm, 10nm, and 7nm node technology. SiBCN is a balanced approach to improving circuit performance and improving yield. SiOCN is also being implemented in 7nm.

Another critical aspect of insulators that affect how they fail is Line Edge Roughness (LER) and random variation in the spacing between neighboring wires. The amount of LER and other random variation is highly dependent on the chip [manufacturing process](#). LER affects the voltage dependence and time dependence of dielectric breakdown. IBM's two papers, *A Stochastic Model for Impact of LER on BEOL TDDDB*, and *A New and Holistic Modelling Approach for Impact of Line-Edge Roughness on Dielectric Reliability* address ways to model LER and other forms of spacing variation to correctly anticipate voltage effects on chip reliability.

Measuring the dielectric breakdown (the point of maximum voltage difference that can be applied across semiconductor insulator materials before the insulator collapses) in the lab, when testing fabricated chips during development, or for final acceptance from the foundry, is a time-consuming process – without knowing in advance which chips will have the shortest lifespans. In the paper, *A Process-Variation-Cognizant Efficient MOL and BEOL TDDDB Evaluation Method*, IBM Systems engineers from the Fabless Reliability Group, with IBM Research engineers, developed a cognitive computing technique for optimal pre-screening and test sequencing to dramatically improve the efficiency of testing.

A different reliability issue concerning the long-term threshold voltage instability of transistors is the subject of extensive research in the paper, *Comparison of DC and AC NBTI Kinetics in Si and SiGe p-FinFETs*. In collaboration with IIT Bombay, IBM Research engineers have performed a comparison of the frequency, voltage, time, and temperature dependence of this phenomenon in traditional Silicon-channel MOSFETs and new [SiGe-channel devices](#).

"The chip needs to be stable at normal operating conditions (about 1 V, and up to 125C for most applications), so the data at higher extremes are used to extrapolate to use condition," Stathis said. "In addition, for this work we tested at frequencies up to 1MHz. While this is far from the chip operation condition (>GHz), it is used to provide information about the NBTI mechanisms which are still very much debated."

The understanding will be crucial in assuring the reliability of these new devices for future technology nodes.

IBM Research Papers at IRPS

Time Dependent Dielectric Breakdown of SiN, SiBCN and SiOCN spacer dielectric

R.G. Southwick III, E. Wu, S. Mehta, J.H. Stathis

A Stochastic Model for Impact of LER on BEOL TDDB

R. Muralidhar, E. Wu, T. Shaw, A. Kim, B. Li, P. Mclaughlin, J. Stathis and G. Bonilla

A Process-Variation-Cognizant Efficient MOL and BEOL TDDB Evaluation Method

Andrew Kim, Ron Bolam, Baozhen Li, Barry Linder, and Ernest Wu

Comparison of DC and AC NBTI Kinetics in Si and SiGe p-FinFETs

Narendra Parihar, Richard G. Southwick, Uma Sharma (IIT Bombay), Miaomiao Wang, James H Stathis and Souvik Mahapatra (IT Bombay)

A New and Holistic Modelling Approach for Impact of Line-Edge Roughness on Dielectric Reliability

E. Wu, R. Muralidhar, T. Shaw, Baozhen, A. Kim, J. Stathis, and G. Bonilla

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